

MS-7175

Version 0A

Intel (R) Grantsdale (GMCH) + ICH6 Chipset
Intel Tejas & Prescott LGA775 Processor

CPU:

Intel Tejas/Prescott - 3.6G

System Chipset:

Intel Grantsdale - GMCH (North Bridge)
Intel ICH6 (South Bridge)

On Board Chipset:

BIOS -- FWH FLASH 4Mb
Azalia Codec -- ALC880
LPC Super I/O -- WINBOND83627THF
LAN-INTEL 10/100 PHY 82562EZ
INTEL GIGA (PCI) 82541GI
CLOCK -- ICS954119
1394 -- VIA VT-6307
H/W Monitor W83792AD

Main Memory:

2 CHANNEL DDR 2 * 4 (Max 4GB)


Expansion Slots:

PCI Express X16 SLOT * 1
PCI 1.2.3 SLOT * 3

Intersil PWM:

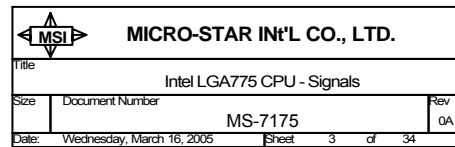
Controller: HIP6565ACV
Driver: HIP6602B + HIP6601B

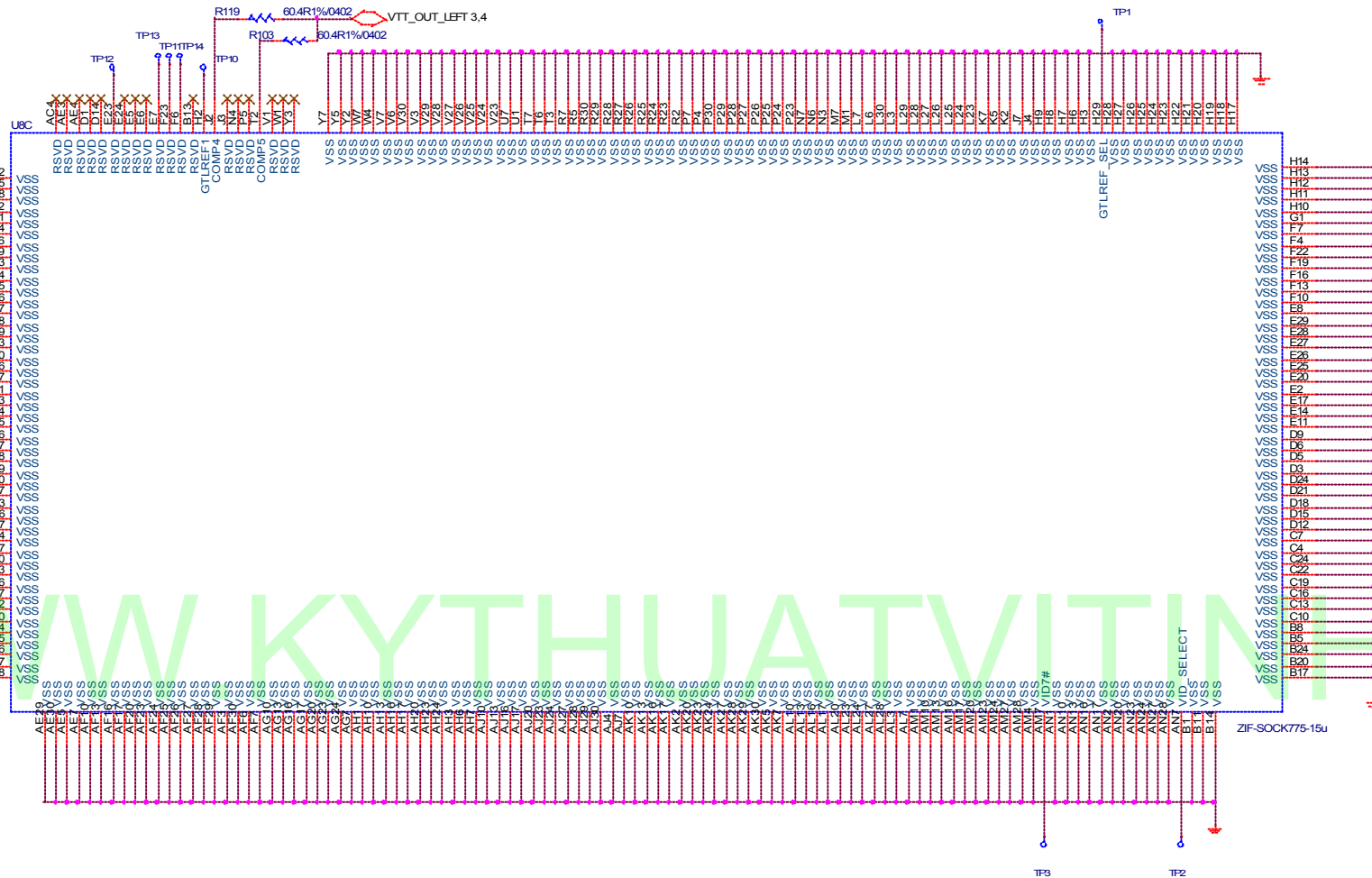
Cover Sheet, Block diagram	1-2
Intel LGA775 CPU - Signals	3
Intel LGA775 CPU - Power	4
Intel LGA775 CPU- GND	5
Intel Grantsdale - CPU	6
Intel Grantsdale - Memory	7
Intel Grantsdale - PCI Express	8
Intel Grantsdale - GND	9
ICH6	10-12
CLOCK - ICS954119	13
LPC I/O - WINBOND83627THF KB/MS	14
FWH/FAN/SERIAL-ATA	15
LAN INTEL 82562EZ & 82541GI	16
LAN CONNECTOR RJ45	17
Azalia CODEC(ALC880)	18
PCIE X16 SLOT & H/W Monitor W83792AD	19
DDR1 DIMM 1 , 2 , 3 & 4	20-22
PCI SLOT 1 & 2 & 3	23
ATX & Front Panel & IDE CONNECTOR	24
USB Connectors	25
IEEE1394-VIA6307	26
MS7 ACPI Controller	27
GPIO & JUMPER SETTING	28
VRM 10 - Intersil HIP 6561 3 phase	29
VGA Connector	30
Revision History	31
Manual Parts & Power Delivery	32

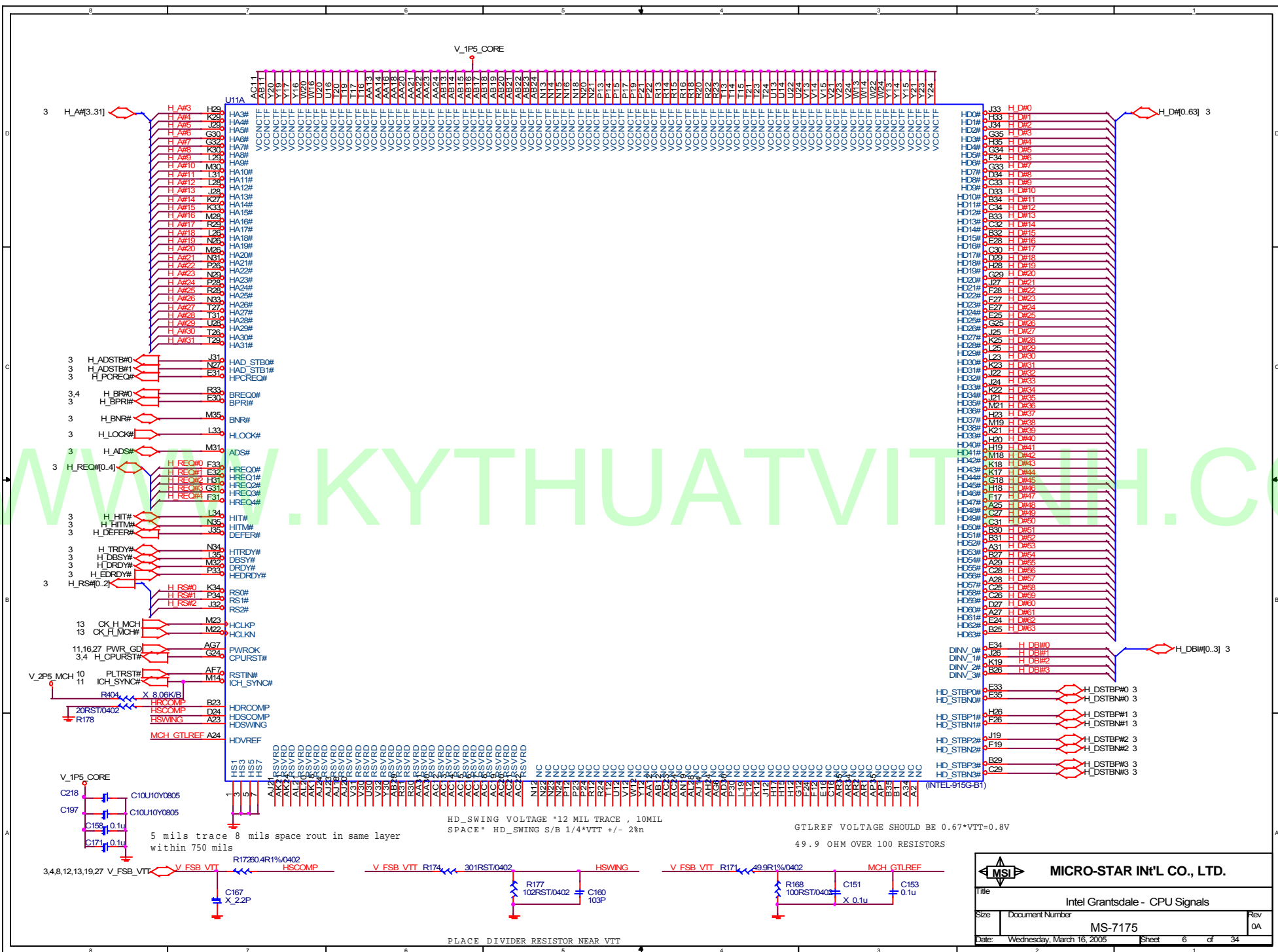
 MICRO-STAR INT'L CO., LTD.	
Title COVER SHEET	
Size	Document Number MS-7175
Date: Wednesday, March 16, 2005	Sheet 1 of 34

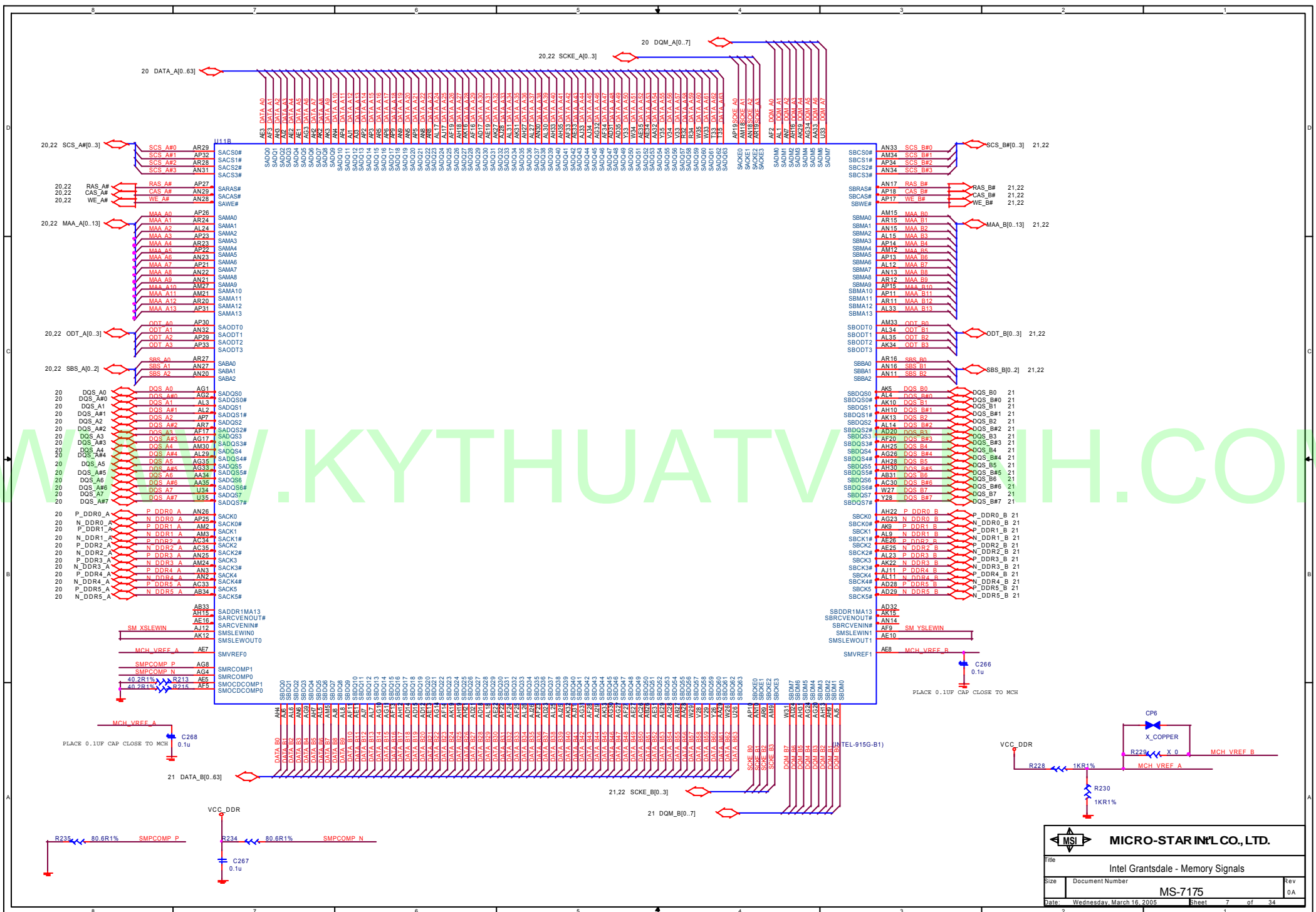
VTT OUT RIGHT			
	RN7		
	8P4R-680		
VID3	1		2
VID1	3		4
VID2	5		6
VID4	7		8
VID0	R81		680/0402
VID5	R84		680/0402

6 H_A#[3.31]






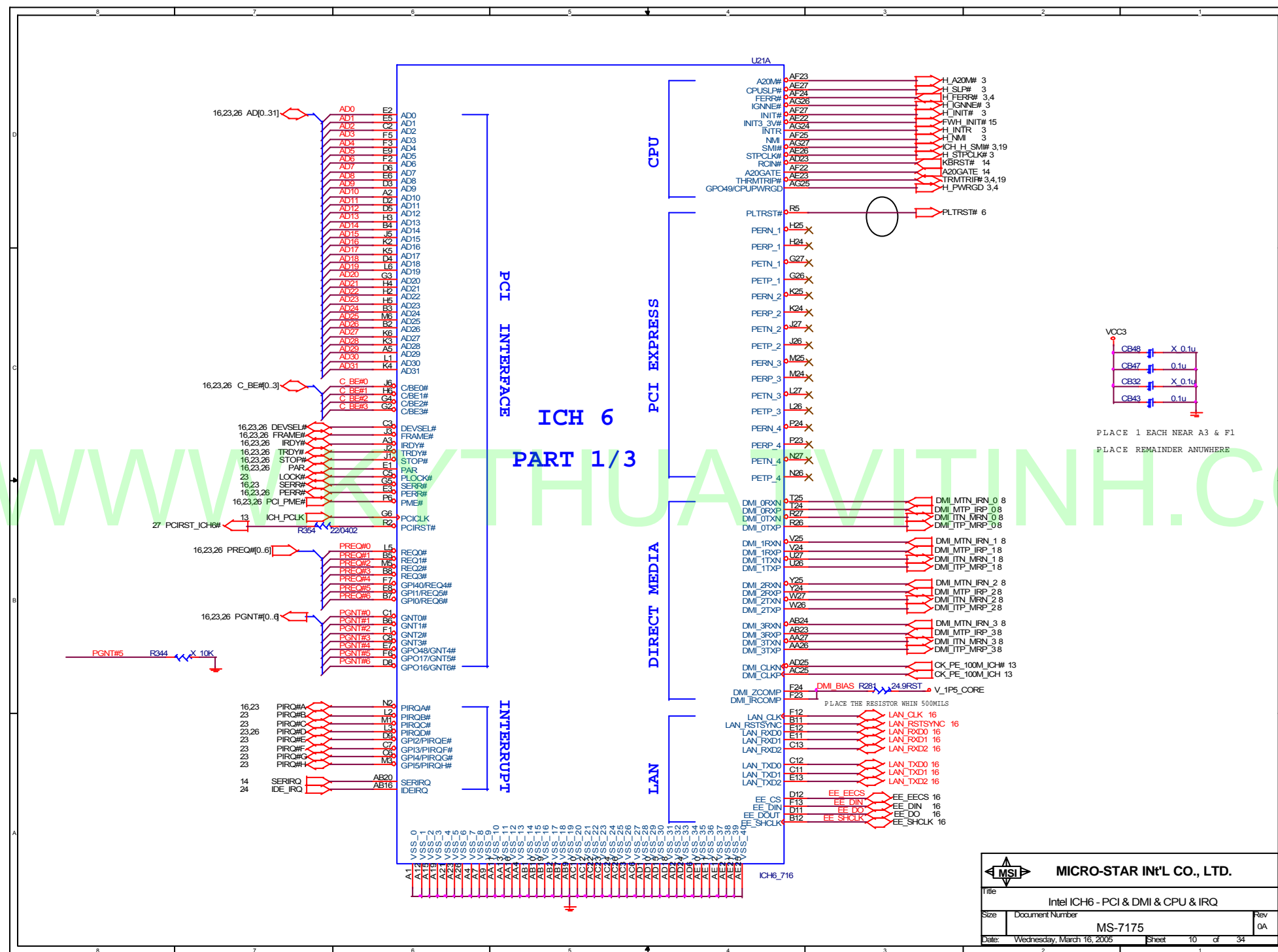




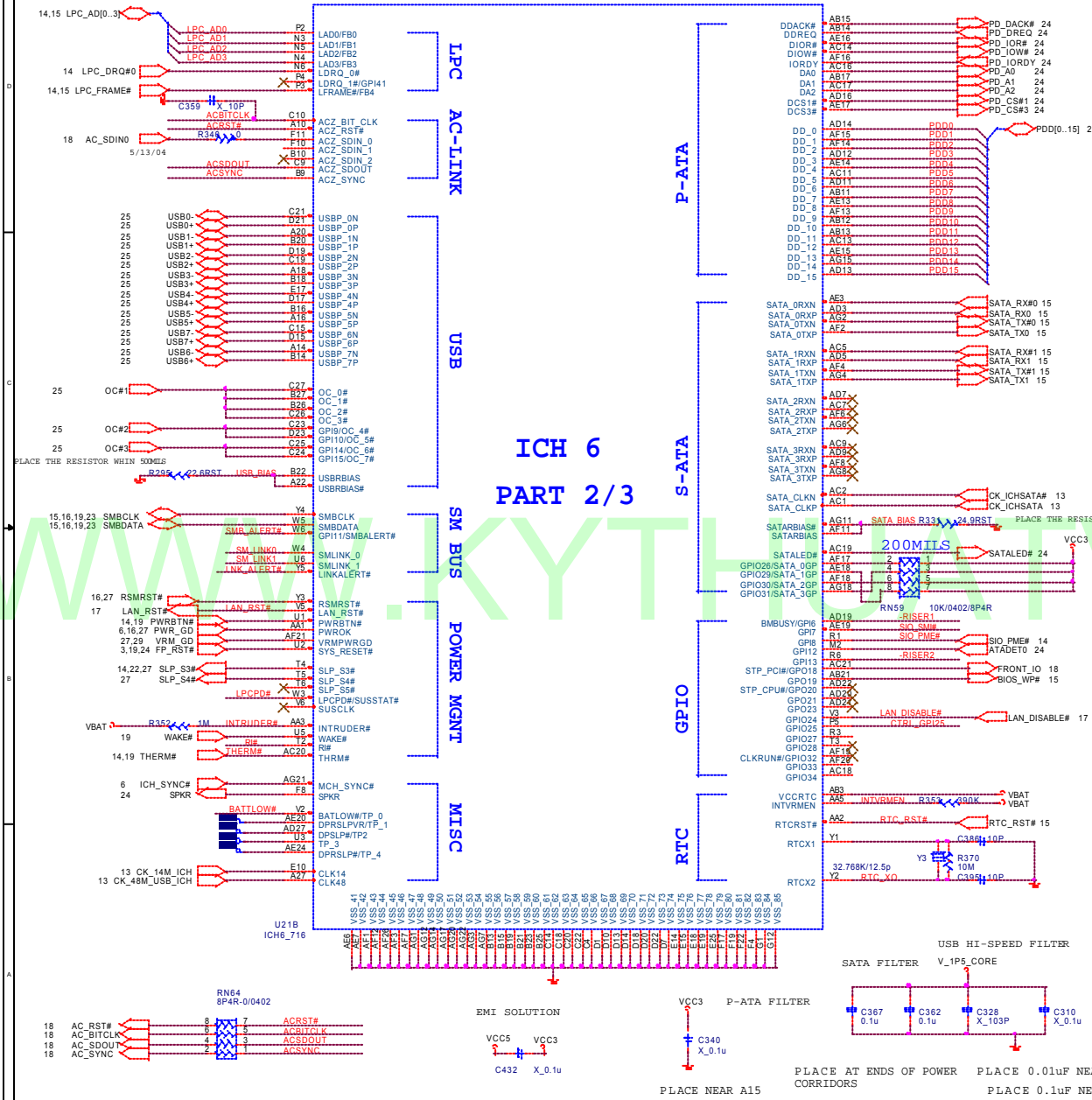


(INTEL 915G-B1)

		MICRO-STAR INT'L CO., LTD.	
Title Intel Grantsdale - GND			
Size	Document Number		Rev DA
MS-7175			
Date: Wednesday, March 16, 2005	Sheet	9	of 34

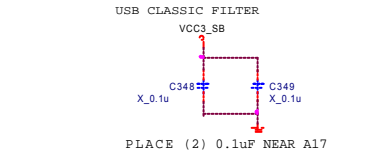
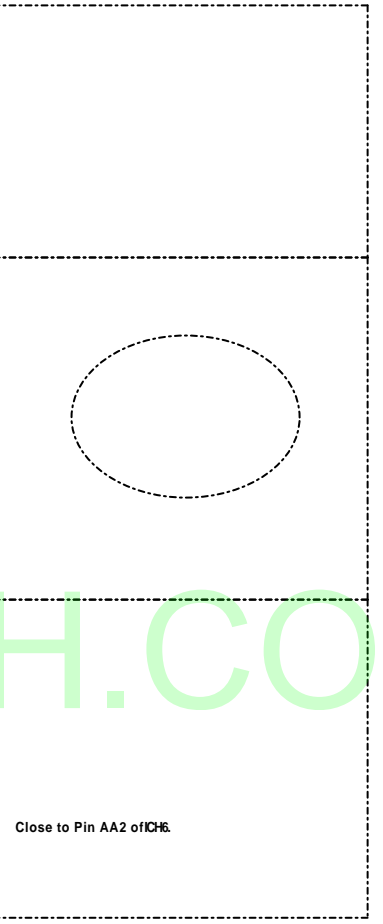
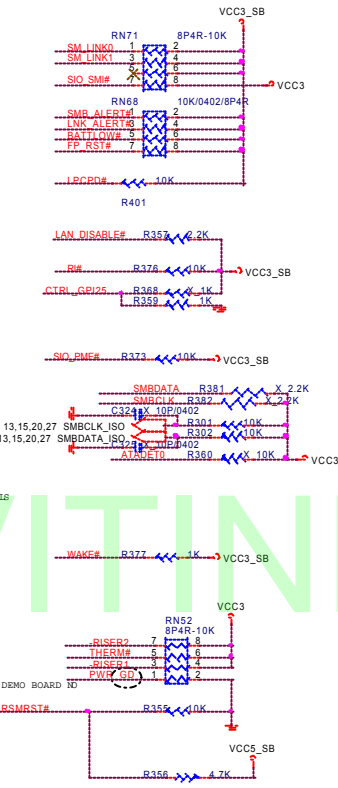


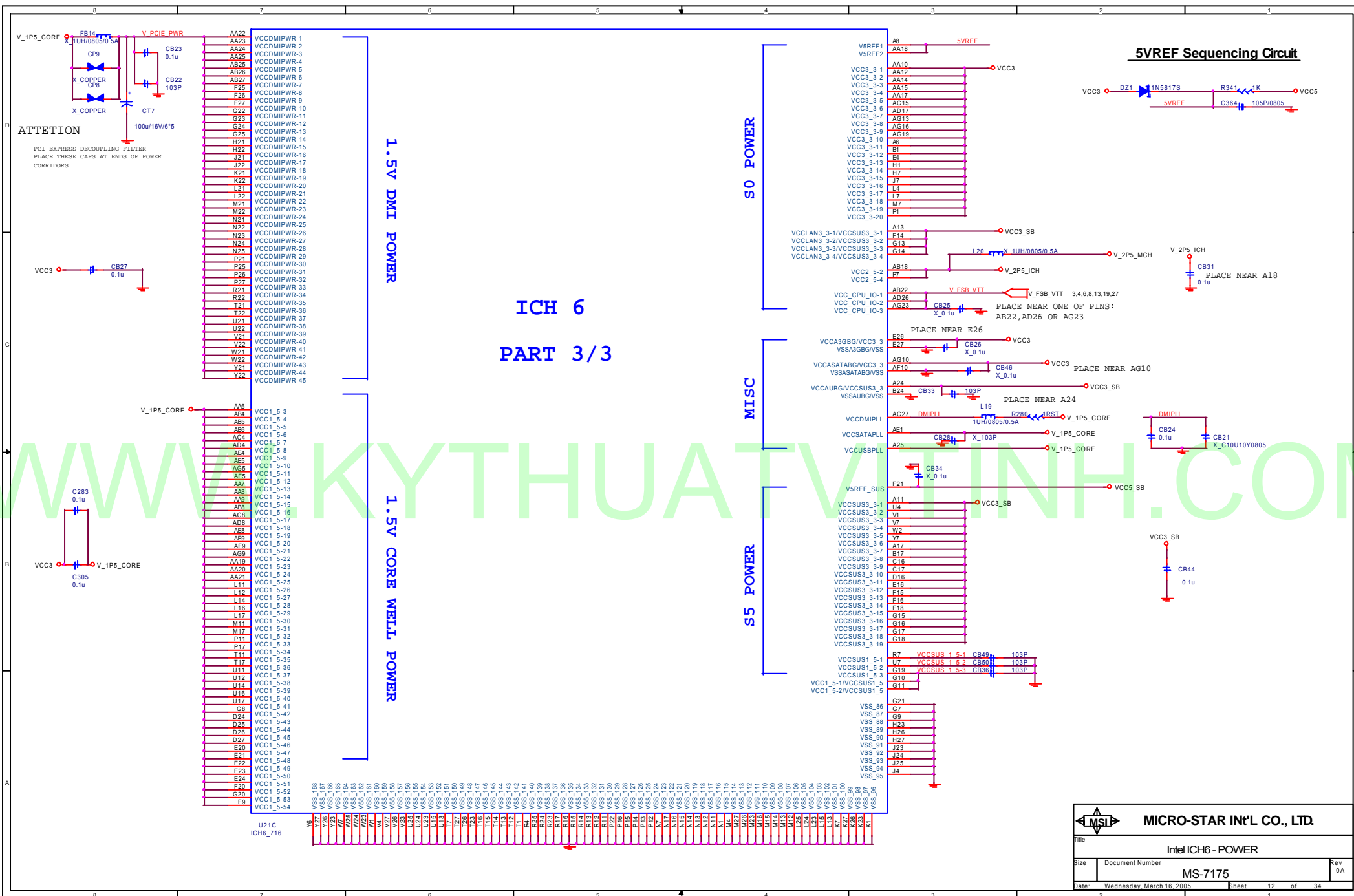
ICH 6
PART 2/3

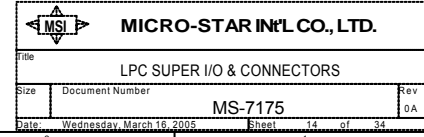


ICH6 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH6
Trace length is less than 3inches to ICH6.

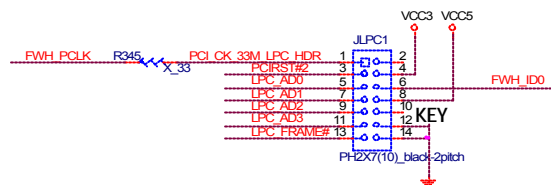




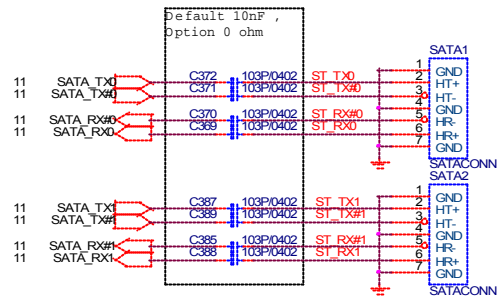


LPC Debug Port

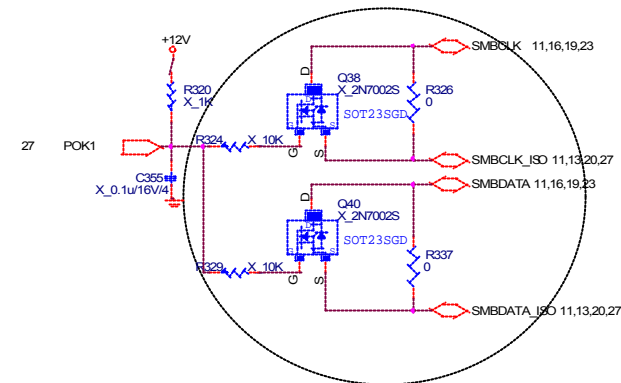
If you place the jumper very closed to FWH bios socket, please use the same clock with FWH. But if you can not place it so close, please use another clock to support it.



SERIAL ATA CONNECTOR BLOCK



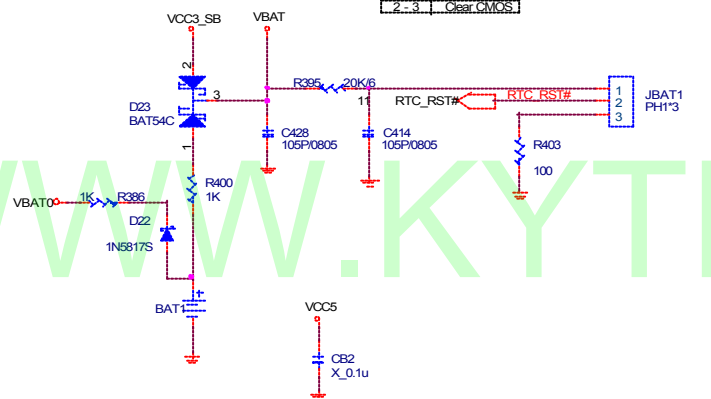
SMBUS ISOLATE



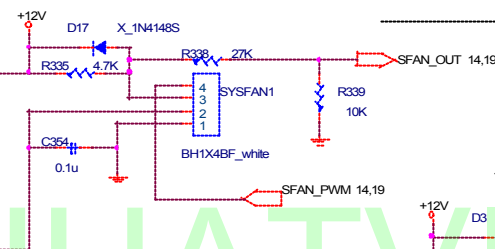
RTC BLOCK

CLR CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

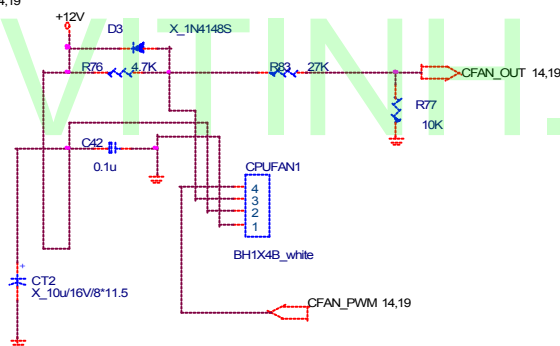
Close to Pin AA2 of ICH6.



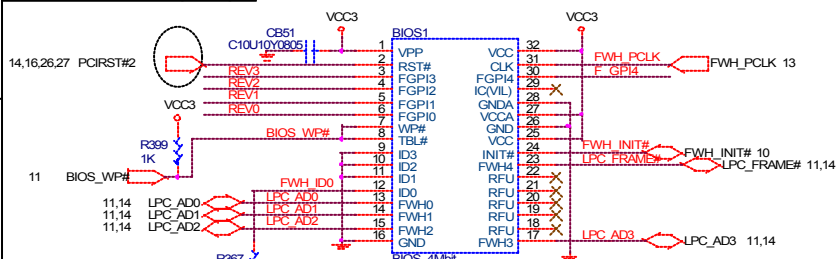
SYSTEM FAN



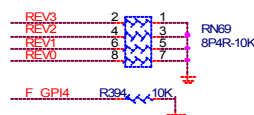
CPU FAN



FIRMWARE HUB (FWH)



FWH RESISTORS



MICRO-STAR INT'L CO., LTD.

Title	FAN, FWH AND SATA
-------	-------------------

Size	Document Number	MS-7175
------	-----------------	---------

Date: Wednesday, March 16, 2005 Sheet 15 of 34

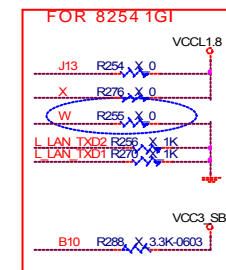
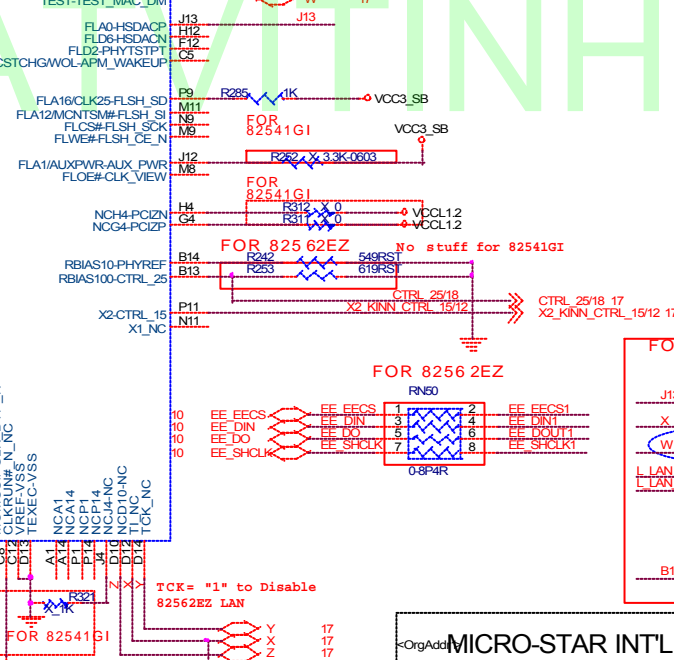
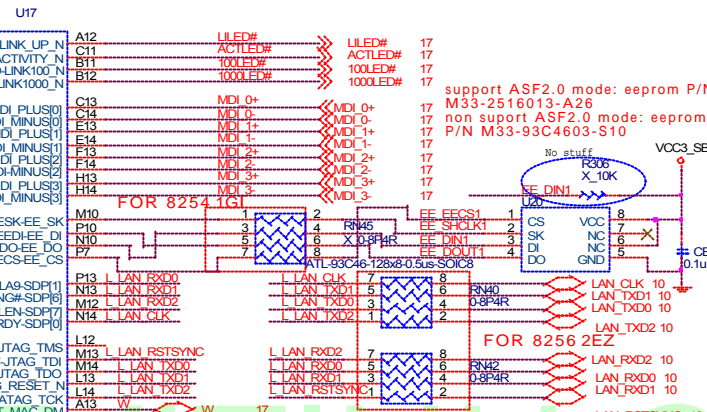
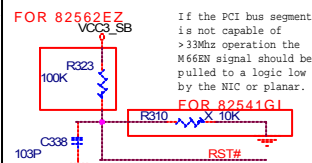
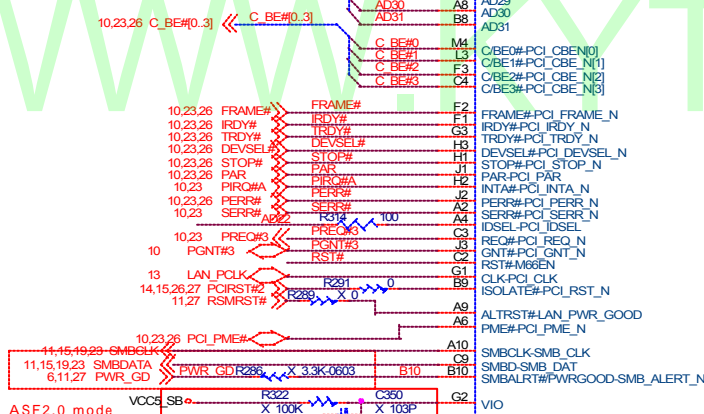
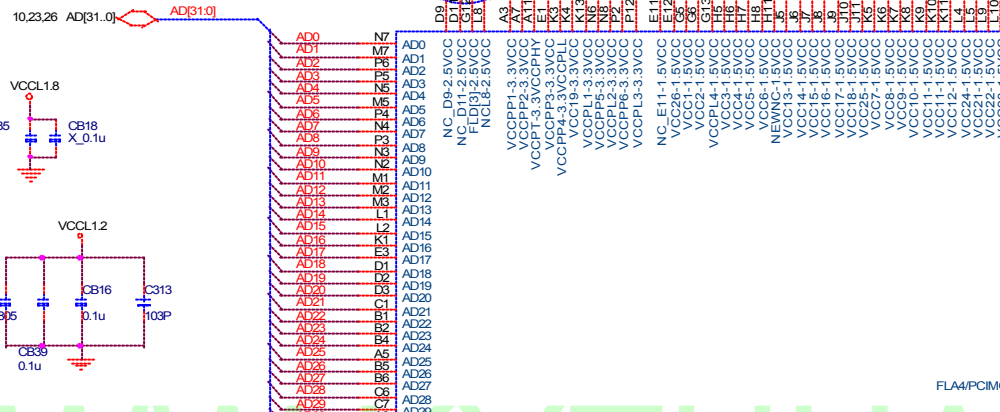
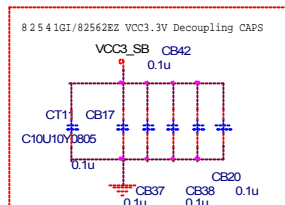
**Gb: Intel 82541GI:
B06-541GI05-I06
10/100: Intel 82562EZ :
B06-562EZ05-I06**



**1.8V RAIL ONLY
REQUIRED WITH 82541GI
CONTROLLER. NOT
CONNECTED WITH
82562EZ**



**1.2V RAIL ONLY
REQUIRED WITH
82541GI
CONTROLLER**

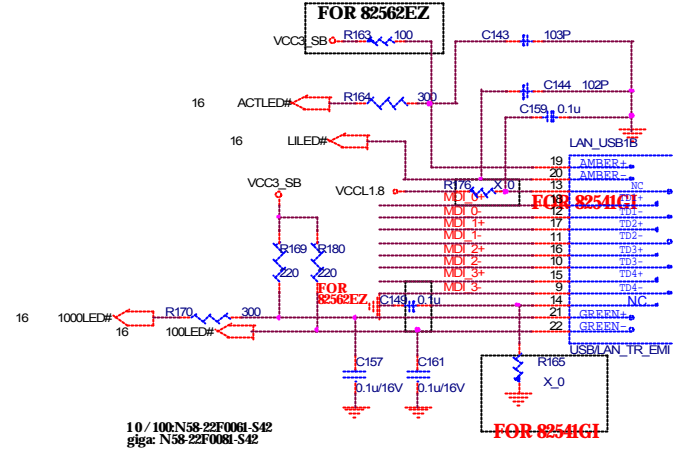
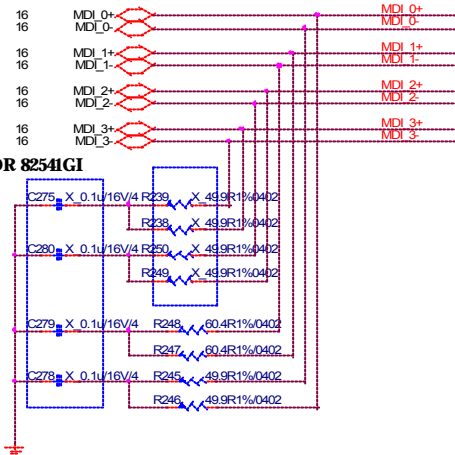


Install pull-down resistor if CLKRUN# is not used.

MICRO-STAR INT'L CO., LTD.

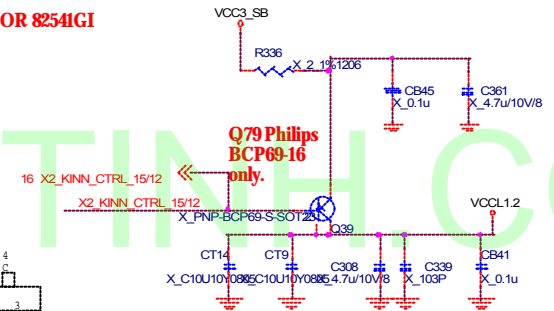
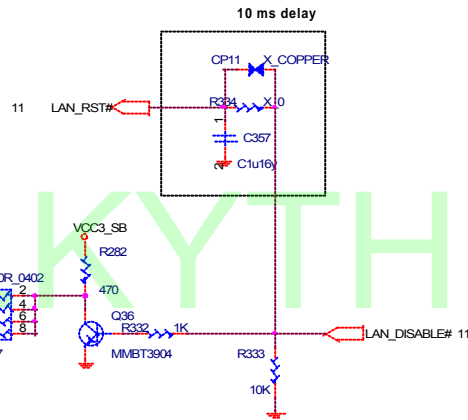
Title			
LAN Intel 82562EZ(10/100) / 82541EI(Giga)			
Size	Document Number		Rev
	MS-7175		()
Date	Wednesday, March 16, 2005	Sheet	16 of 34

FOR 8254IGI

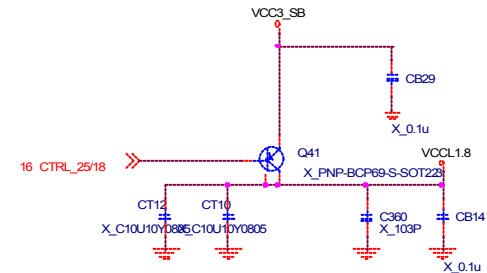


10/100N58-22F0081-S42
giga: N58-22F0081-S42

FOR 8254IGI

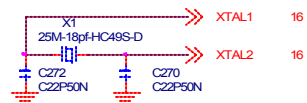


INSTALL POWER TRANSISTOR Q79 & Q80 AND SUPPORT COMPONENTS ONLY WHEN USING KENAI32 CONTROLLER

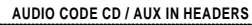


LAN Crystal

THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.



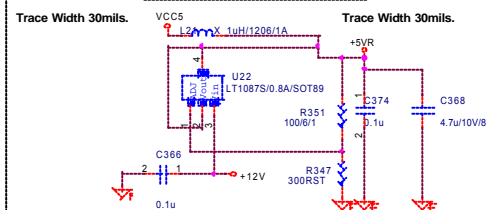
<OrgAddr> MICRO-STAR INT'L CO., LTD.			
Title LAN CONTROLLER			
Size	Document Number	Rev	
	MS-7175	0A	
Date: Wednesday, March 16, 2005	Sheet	17	of 34



For E

CP16 X

AUDIO CODE REGULATORS



Place those component close to audio connector.

Place those component close to
audio connector.

VCC5

CP12

1

2

X_COPPER

C18

X 0.1u

SPDIF0

L22

1

2

X_301/6

560P

C373

1

2

VCC

SPDIF_OUT

20

19

21

GND

GND

GND

AUDIO1F

CONN-AUDIOJACKX5_SPDIFX1-10u-1

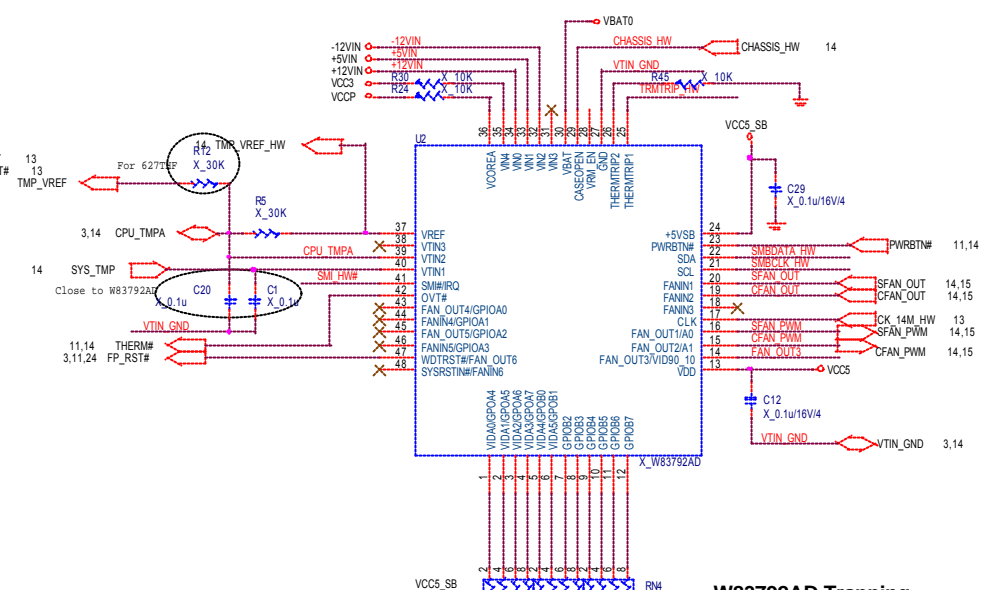
[illegible]

The diagram illustrates the front panel connector wiring. It shows two main signal paths: SENSE A and SENSE B. SENSE A is connected to pins R369, R372, R358, and R362. These pins are connected to components: 5.1KST, 10K/1%, 20K/6/1, and 39.2K/6/1 respectively. The components are then connected to FRONT_ID, LINE1_ID, MIC1_ID, and SUBB_ID. SENSE B is connected to pin R389, which is connected to 10K/1%, and then to CEN_ID and AZ_FRONT_ID.

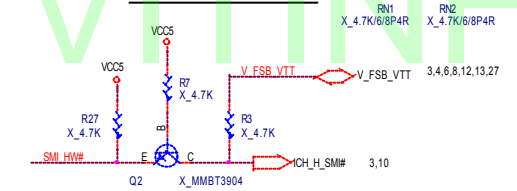
Title	Azalia & Interanal SPK		Rev
Document Number	MS-7175		0A
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, March 16, 2005	
		Sheet 18 of 34	



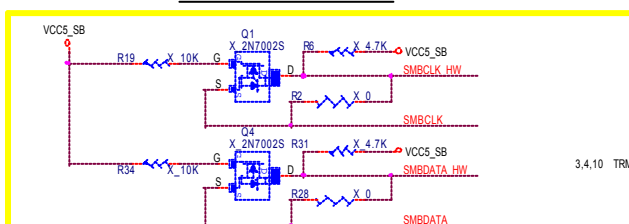
W83792AD H/W MONITOR



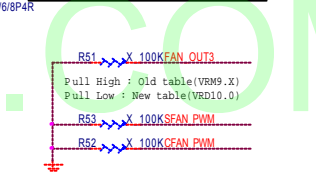
SMI# Level Shift



SM-BUS Level Shift

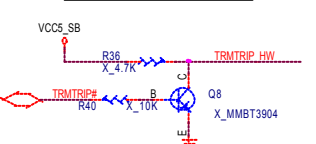


W83792AD Trapping

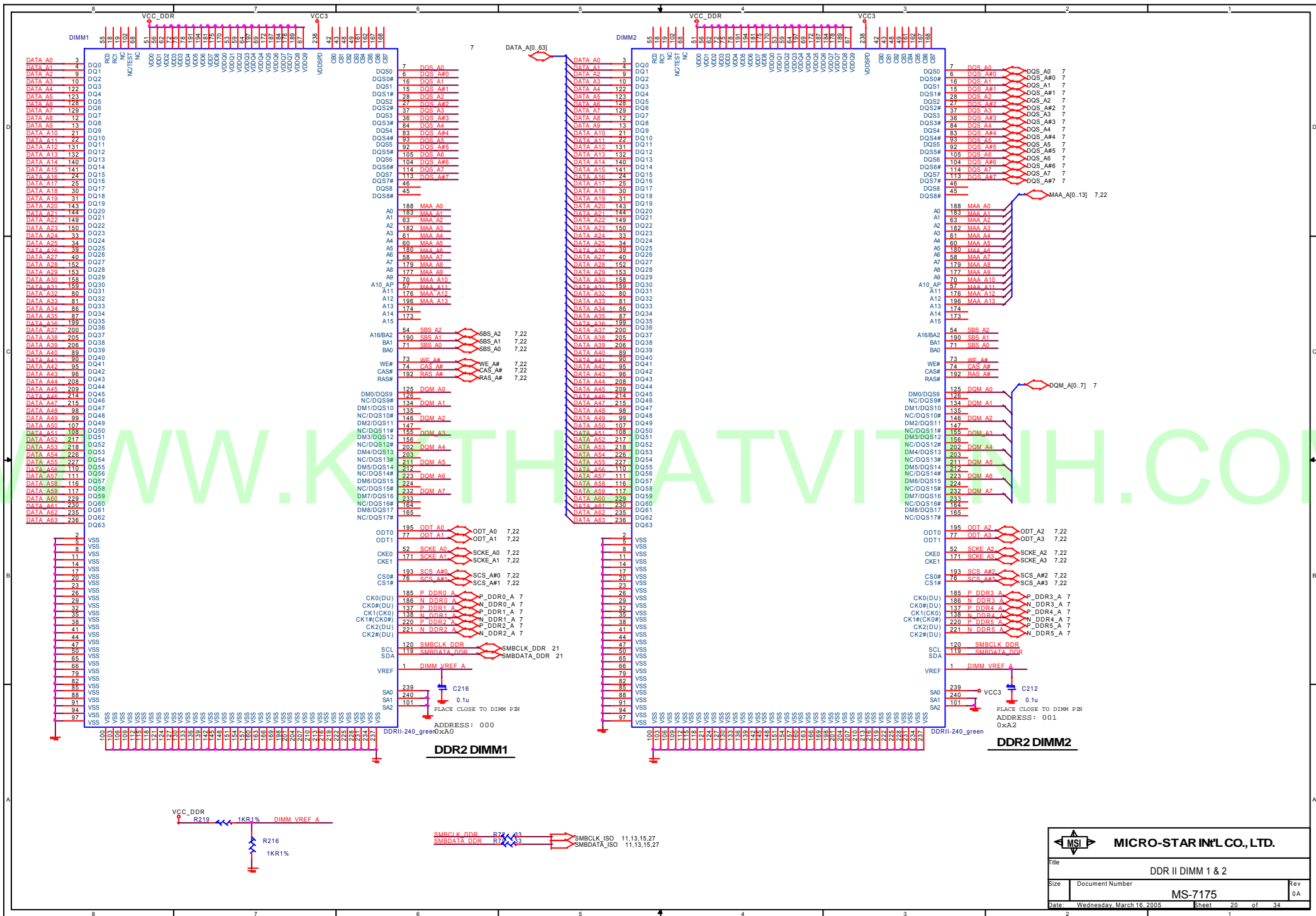


	CFAN_PWM (A1=0)	CFAN_PWM (A1=1)
SFAN_PWM (A0=0)	792D (0x58) T2 (0x90) T3 (0x98)	792D (0x5C) T2 (0x94) T3 (0x9C)
SFAN_PWM (A0=1)	792D (0x5A) T2 (0x92) T3 (0x9A)	792D (0x5E) T2 (0x96) T3 (0x9E)

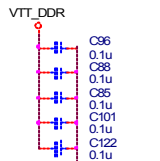
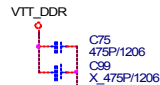
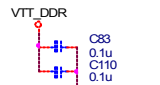
TRMTRIP# Circuit



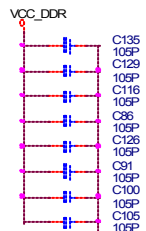
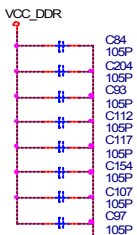
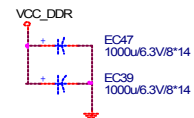
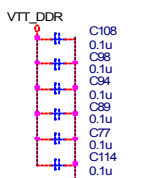
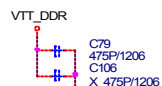
**MECHANICAL
ISSUE
PLACE
ABOVE PCIE**



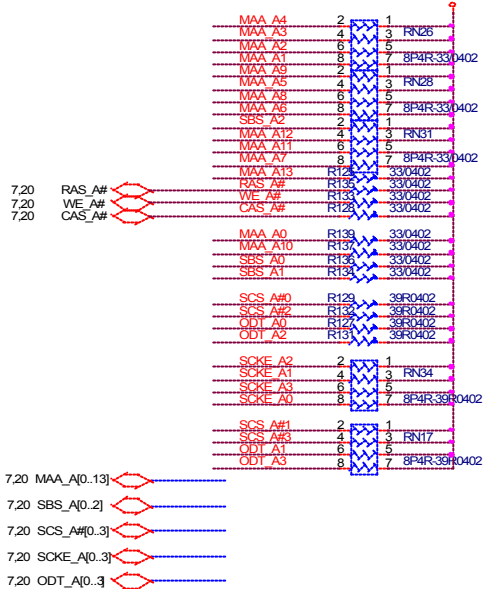
CHANNEL A V_{SM_VTT} DECOUPLING CAPS



CHANNEL B V_{SM_VTT} DECOUPLING CAPS



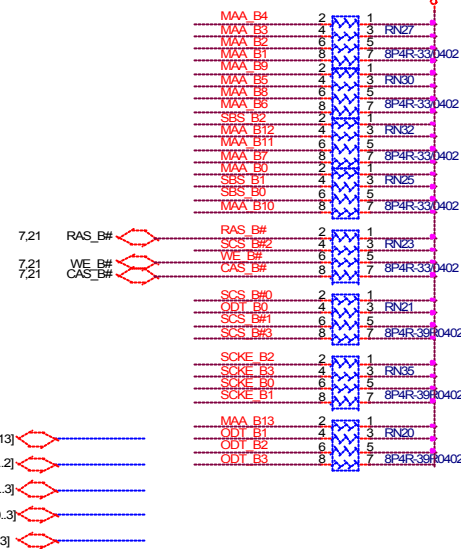
VTT_DDR



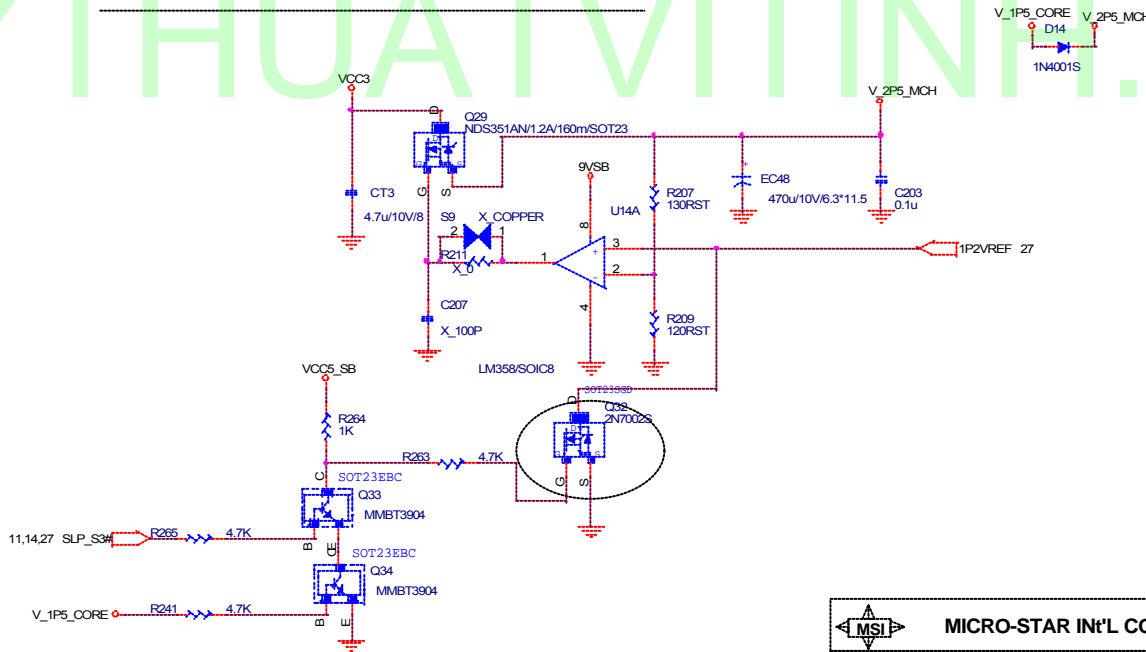
FOR EMI

VCC3 C132 0.1u/10V/6

VTT_DDR

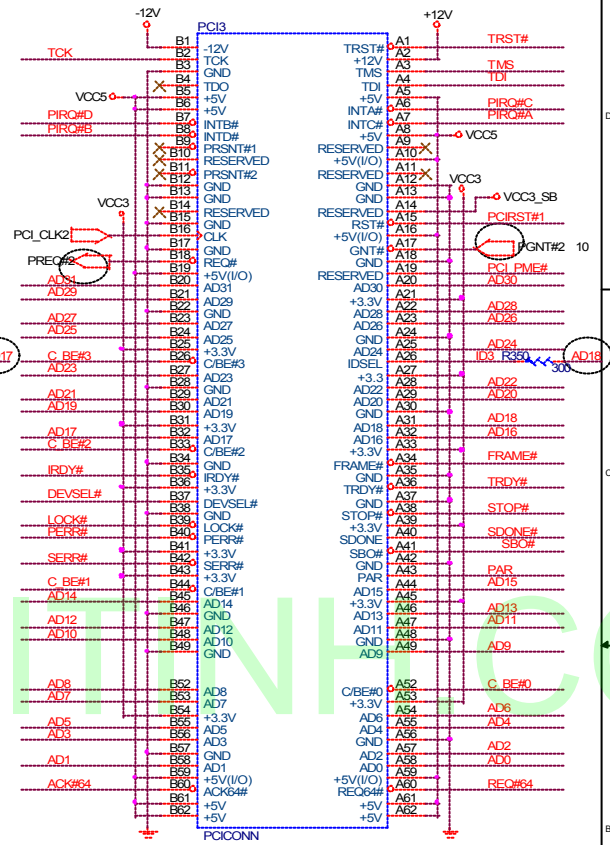


Grantsdale GMCH Power Sequencing Requirement Between 1.5V Core and 2.5V DAC



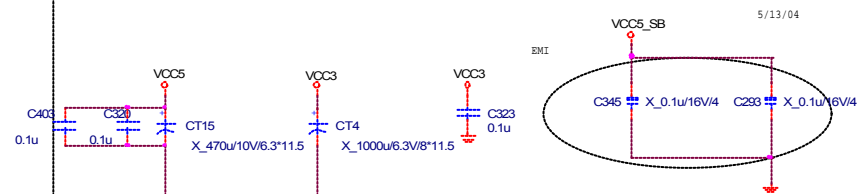
MICRO-STAR INT'L CO., LTD.			
Title: DDR1 VTT DECOUPLING			
Size	Document Number	Rev	
	MS-7175	0A	
Date: Wednesday, March 16, 2005	Sheet	22	of 34

PCI SLOT 3 (PCI VER: 2.2 COMPLY)



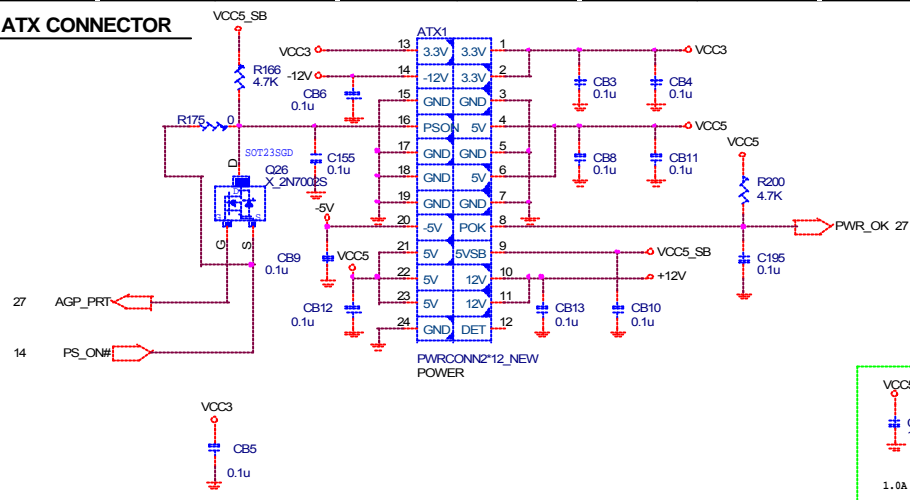
```
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C
```

PCI SLOT DECOUPLING CAPACITORS

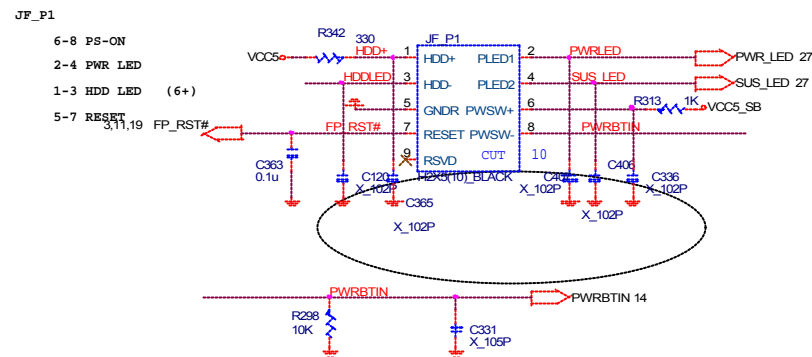


Title				PCI 1&2 & 3 Slots			
Size		Document Number					Rev
		MS-7175					0A
Date:		Wednesday, March 16, 2005		Sheet		23	of 34

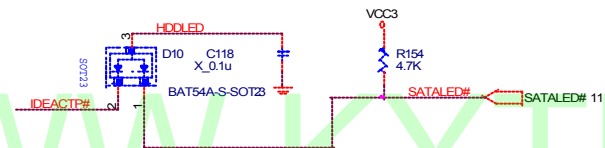
ATX CONNECTOR



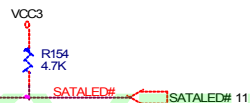
MEDION Front Panel



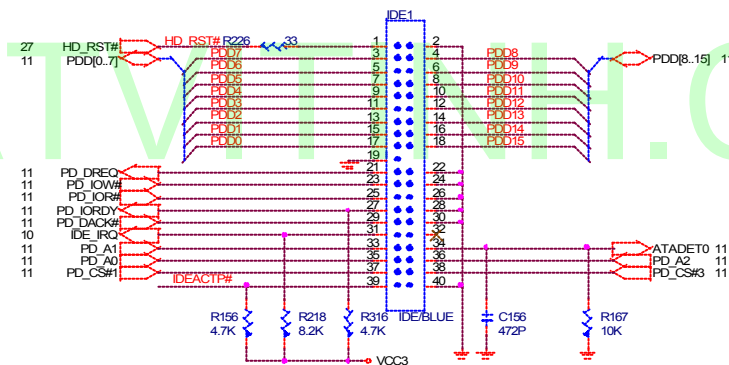
IDE LED



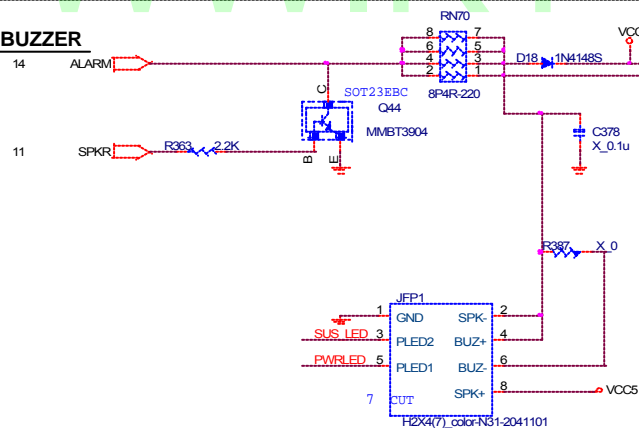
SERIAL ATA LED



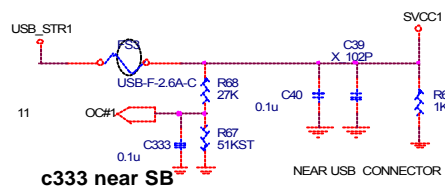
PRIMARY IDE BLOCK



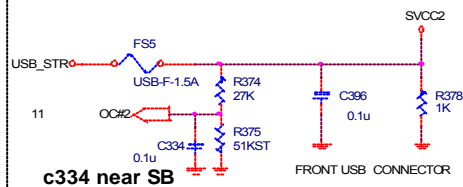
BUZZER



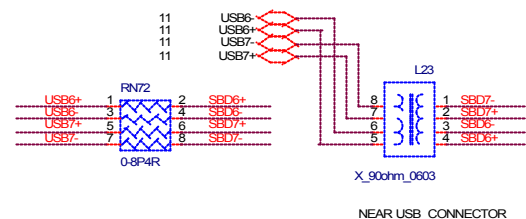
POWER CIRCUIT FOR USB PORT 0,1,2,3



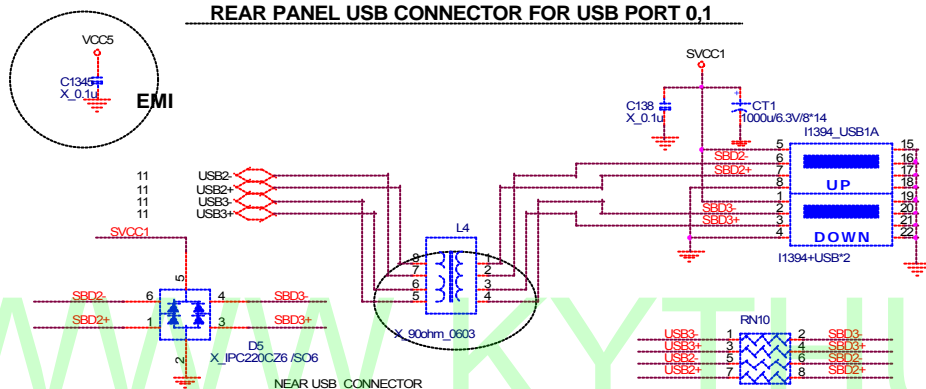
POWER CIRCUIT FOR USB PORT 4,5



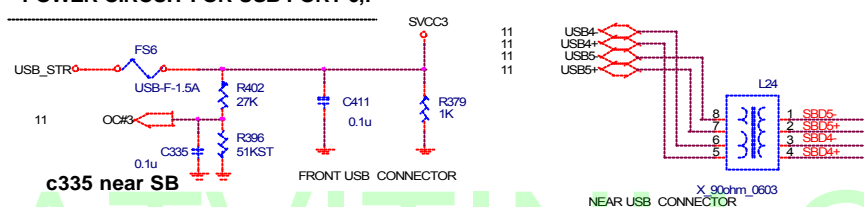
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



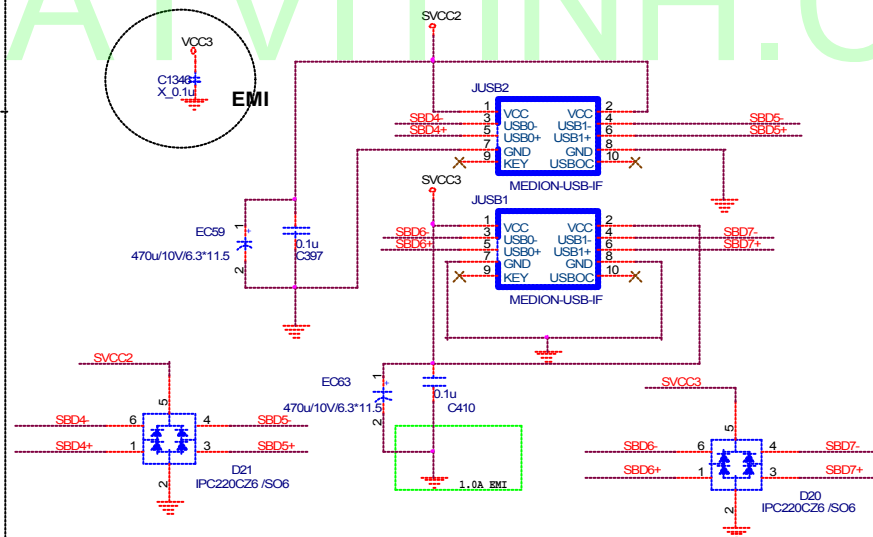
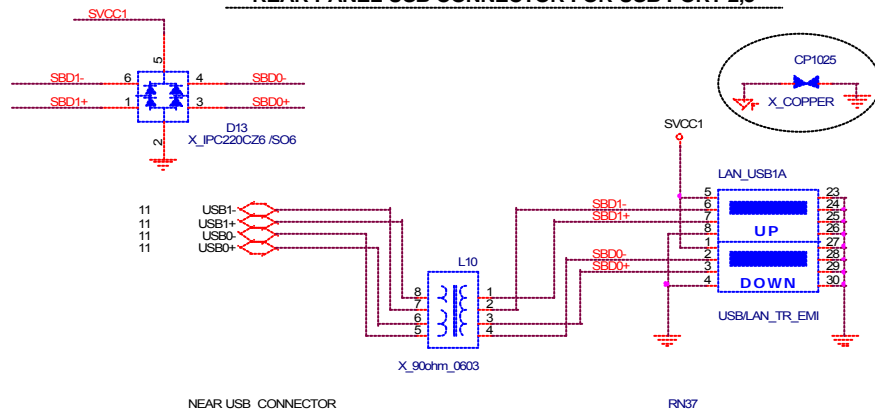
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



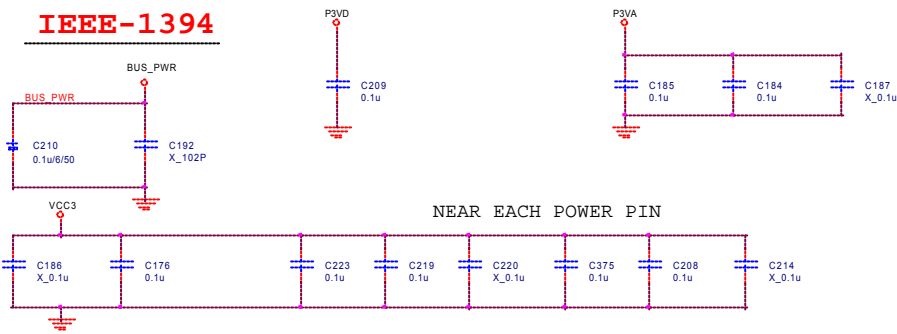
POWER CIRCUIT FOR USB PORT 6,7



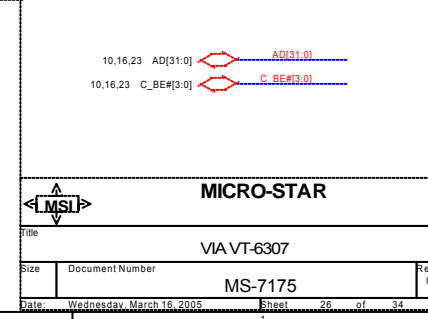
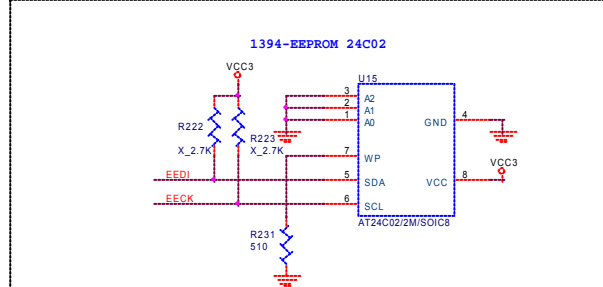
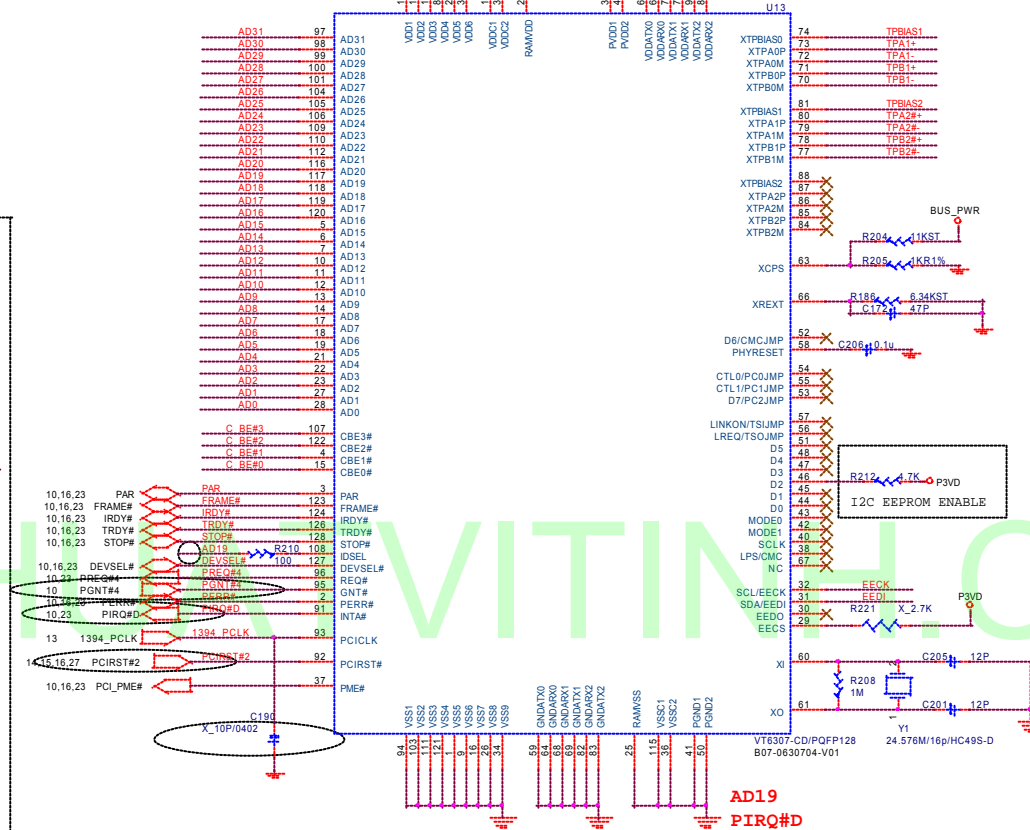
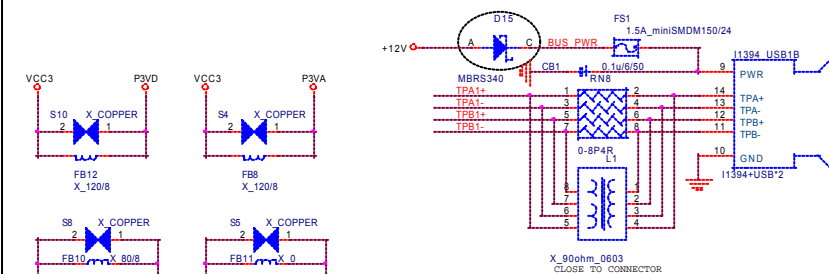
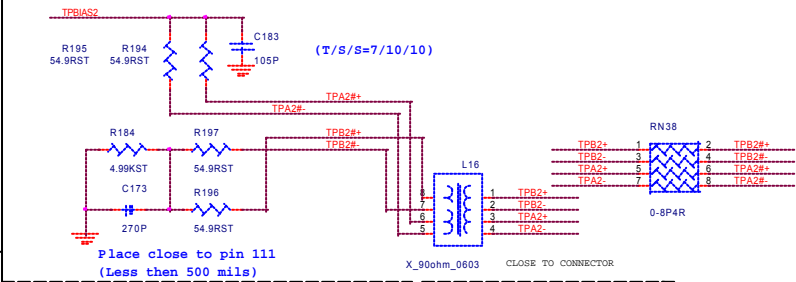
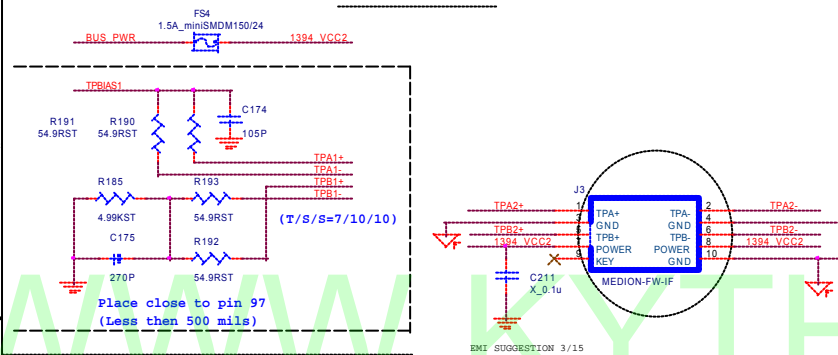
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



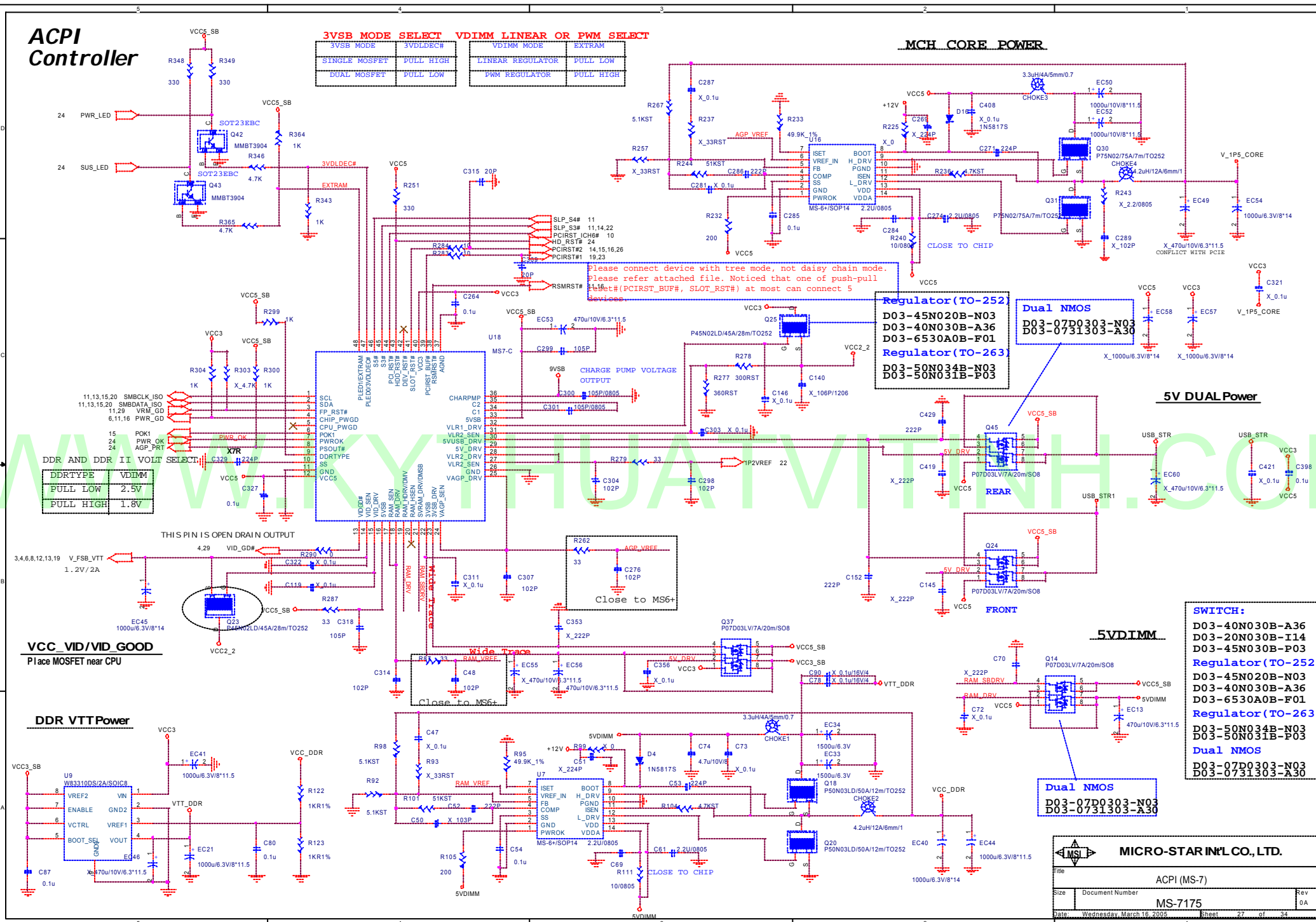
IEEE-1394



FRONT 1394 PORT 1



**ACPI
Controller**



ICH6

GPIO Pin	Type	Function
GPIO 0	I	REQ6# (multifunction pin)
GPIO 1	I	REQ5# (multifunction pin)
GPIO 2	I	PCI_IRQ#E (multifunction pin)
GPIO 3	I	PCI_IRQ#F (multifunction pin)
GPIO 4	I	PCI_IRQ#G (multifunction pin)
GPIO 5	I	PCI_IRQ#H (multifunction pin)
GPIO 6	I	-RISER1 (multifunction pin)
GPIO 7	I	SIO_SMI# (multifunction pin)
GPIO 8	I	SIO_PME# (multifunction pin)
GPIO 9	I	Unused (multifunction pin)
GPIO 10	I	Unused (multifunction pin)
GPIO 11	I	Unused (multifunction pin)
GPIO 12	I	ATADETO
GPIO 13	I	-RISER2
GPIO 14	I	Unused (multifunction pin)
GPIO 15	I	Unused (multifunction pin)
GPIO 16	O	GNT6# (multifunction pin)
GPIO 17	O	GNT5# (multifunction pin)
GPIO 18	O	Unused (multifunction pin)
GPIO 19	O	Unused (multifunction pin)
GPIO 20	O	Unused (multifunction pin)
GPIO 21	O	Unused (multifunction pin)
GPIO 22	OD	Unused (multifunction pin)
GPIO 23	O	Unused (multifunction pin)
GPIO 24	I/O	MB_ID0
GPIO 25	I/O	CTRL_GPI25
GPIO 27	I/O	MB_ID1
GPIO 28	I/O	Password Clear(Active low)
GPIO 32	I/O	(multifunction pin)
GPIO 33	I/O	MB_ID2
GPIO 34	I/O	MB_ID3
GPIO 40	I	PREQ#4 (multifunction pin)
GPIO 41	I	LDRO1 (multifunction pin)
GPIO 48	O	PGNT#4 (multifunction pin)
GPIO 49	OD	CPU_GD (multifunction pin)

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQA PIROB PIROC PIROD	PCI_REQ#0 PCI_GNT#0	AD16	PCI_CLK1
PCI Slot 2	PIROB PIROC PIROD PIRQA	PCI_REQ#1 PCI_GNT#1	AD17	PCI_CLK0
PCI Slot 3	PIROC PIROD PIRQA PIROB	PCI_REQ#2 PCI_GNT#2	AD18	PCI_CLK2
LAN	PIROC	PCI_REQ#6 PCI_GNT#6	AD22	LAN_PCLK
1394	PIROD	PCI_REQ#4 PCI_GNT#4	AD20	1394_PCLK
PCI 2 MASTER	PIROE	PCI_REQ#3 PCI_GNT#3	AD19	PCI_CLK3
IDE RAID	PIROG	PCI_REQ#5 PCI_GNT#5	AD21	RAID_PCLK

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A6H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING


JBAT1	(1 - 2) NORMAL	(2 - 3) CLEAR

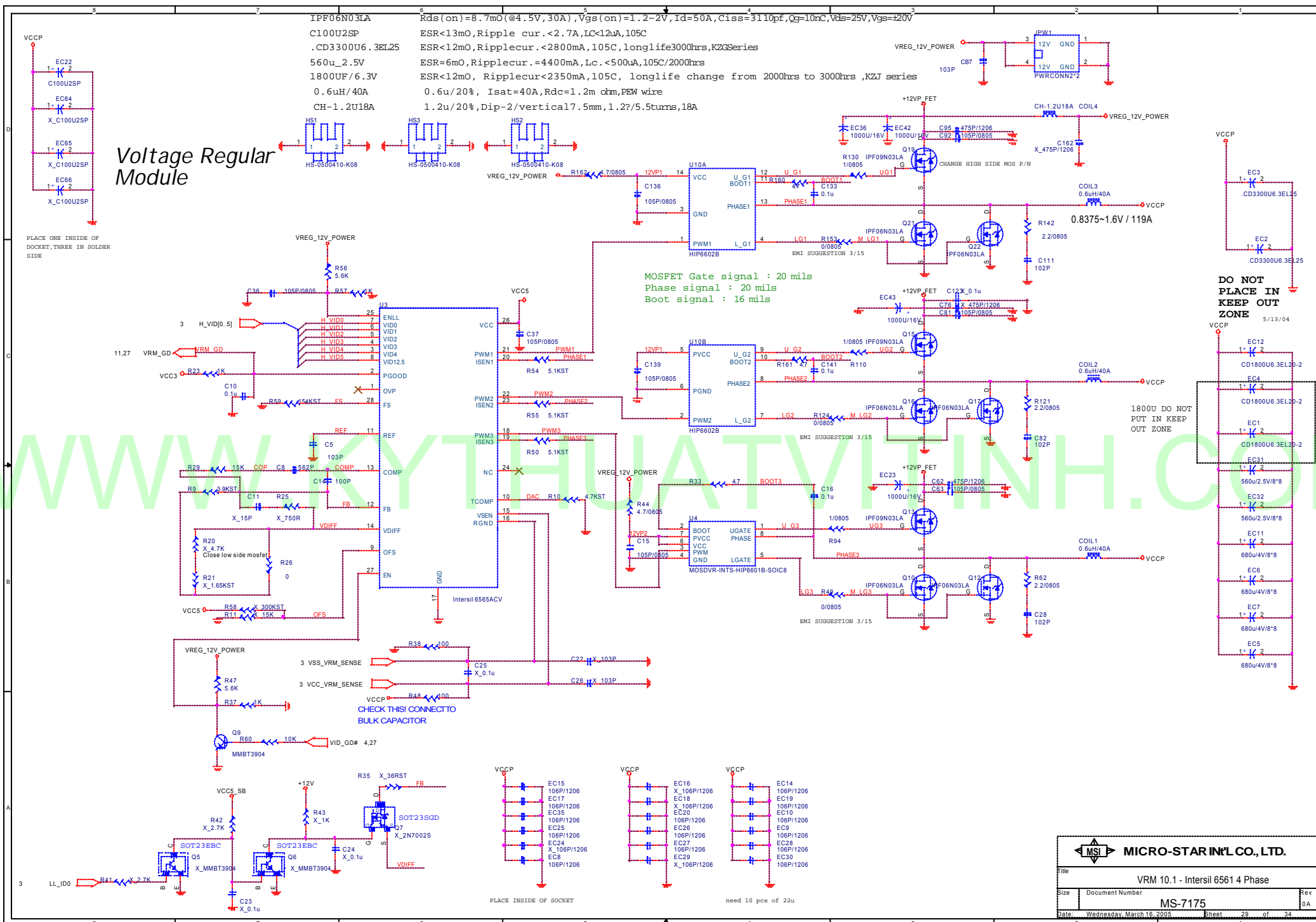
SIO

PIN NAME	USAGE	Input/Output	NOTES
GPIO34	BIOS_WP#	OUTPUT	BIOS Write Protect
GPIO35	2X12_DET	INPUT	2x12 Power Conn Detect

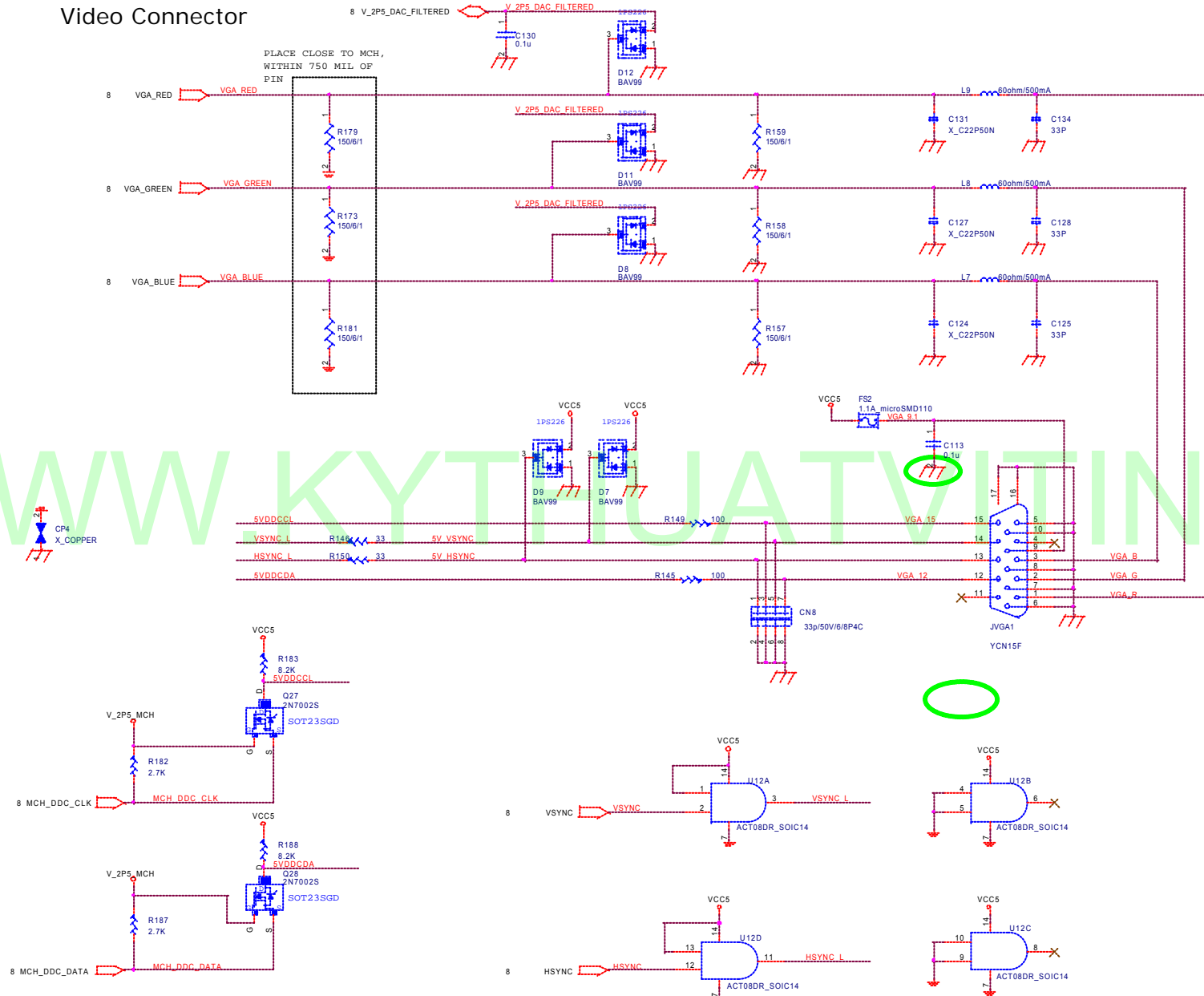
PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI 1-3
PCIRST#2	Super I/O, 1394, LAN, FWLH
PCIRST_ICH6#	PCI-E
HDDRST#	Primary IDE

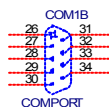
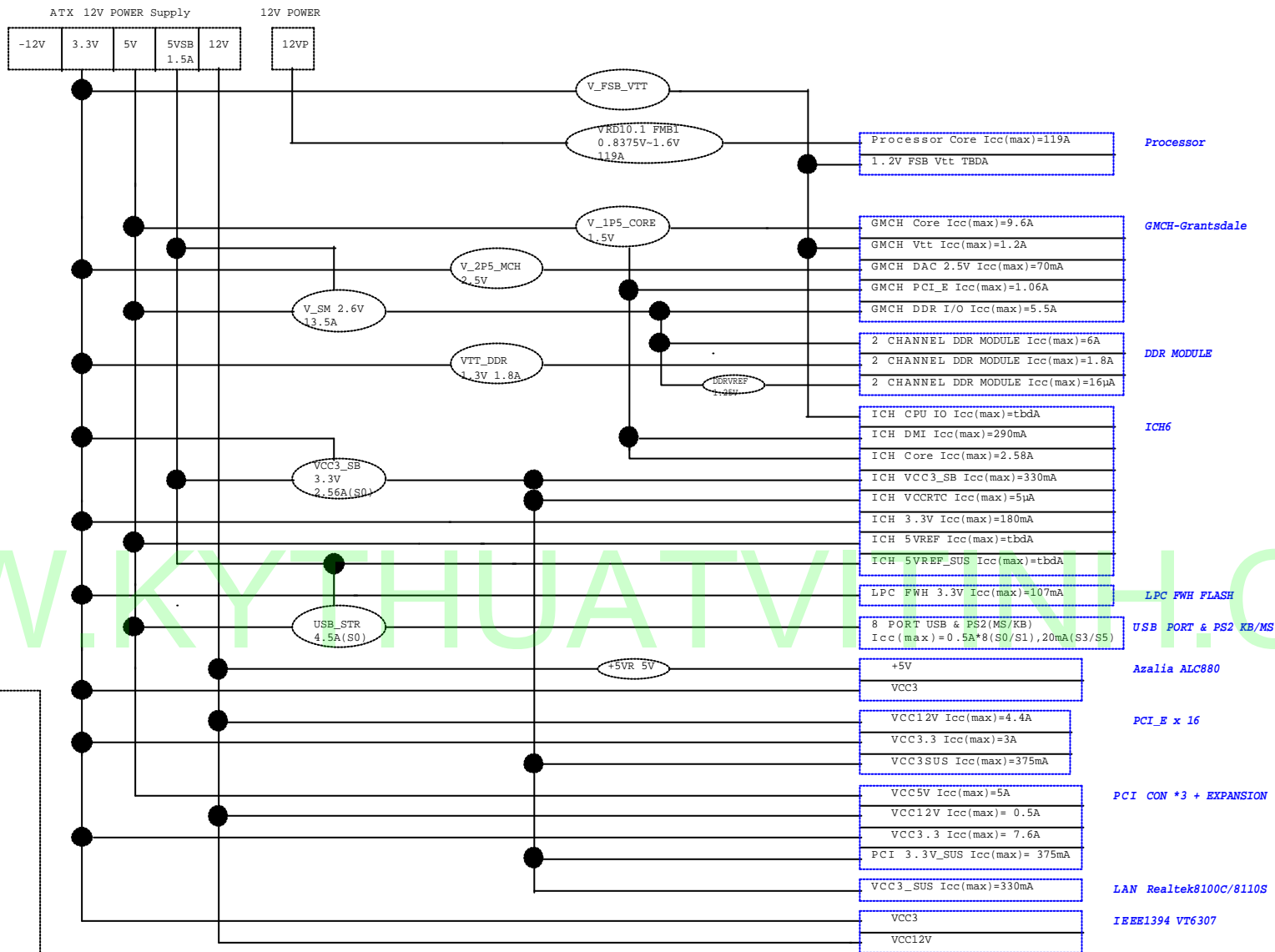
 MICRO-STAR INT'L CO., LTD.	
Title: General Purpose Spec & JUMPER SETTING	
Size: Document Number	Rev: 0A
MS-7175	
Date: Wednesday, March 16, 2005	Sheet: 28 of 34



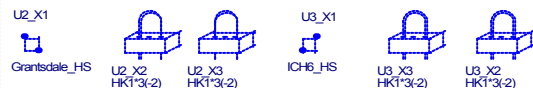
Video Connector



POWER DELIVERY MAP



HEAT SINK

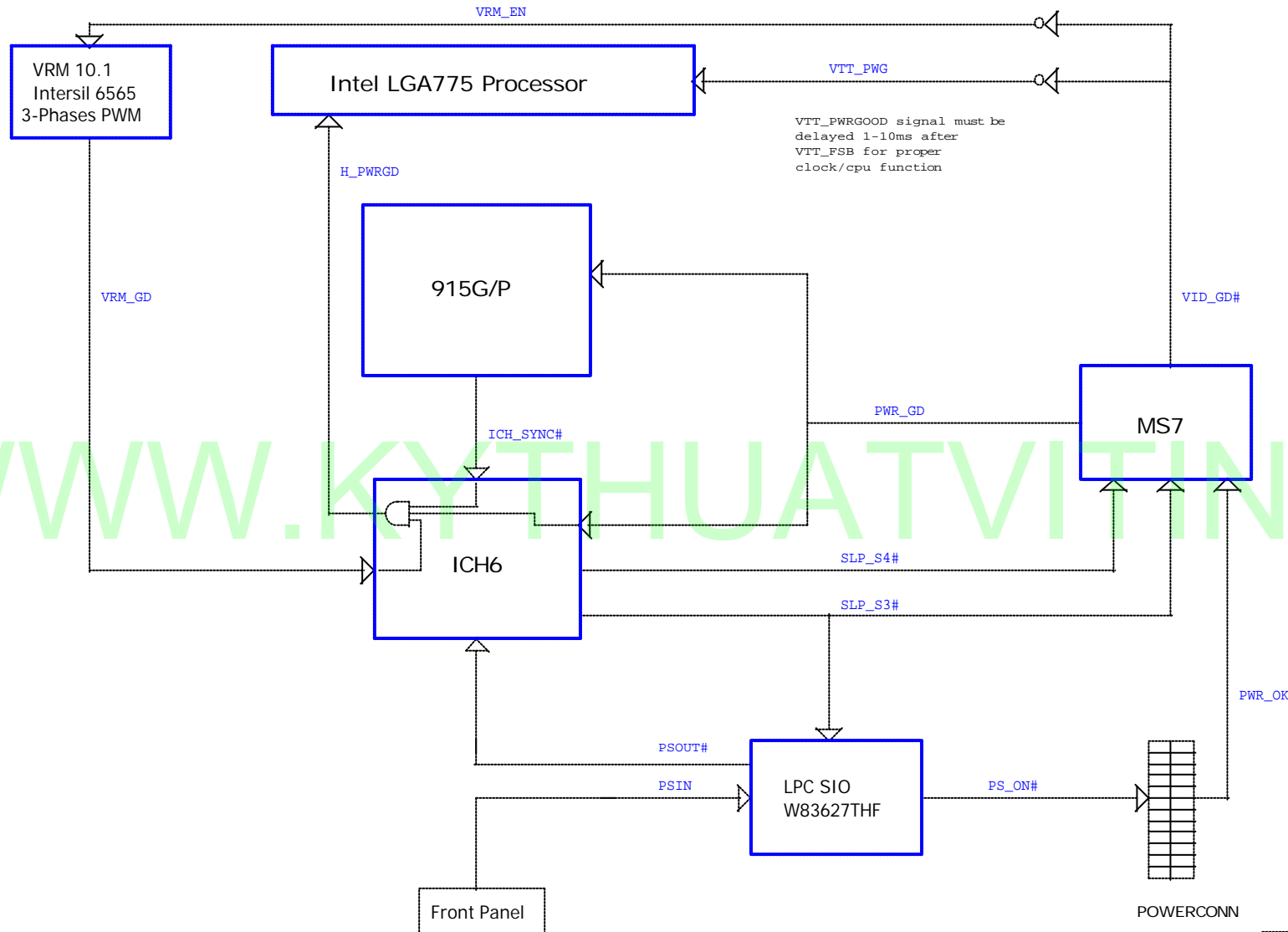


MANUAL PART

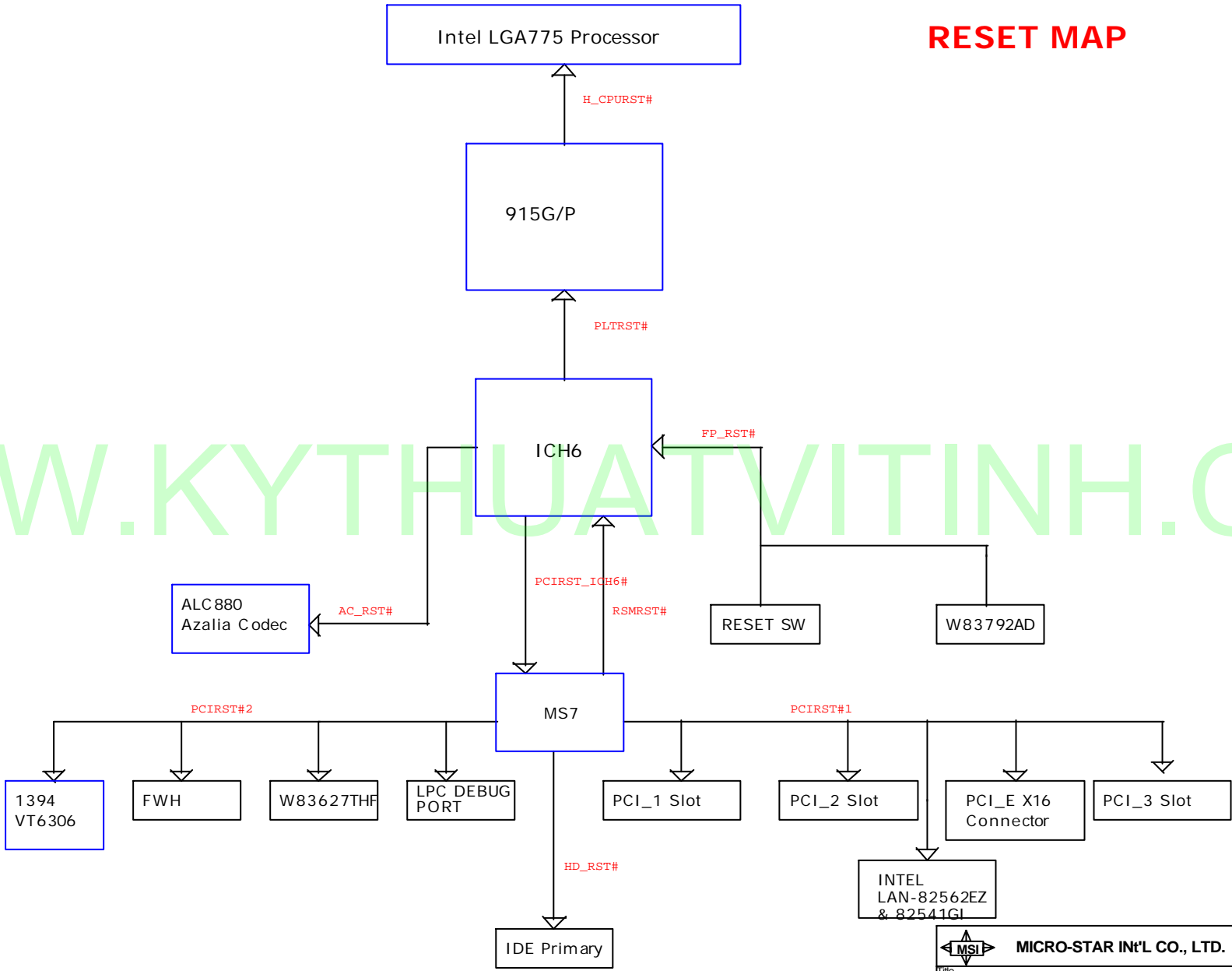


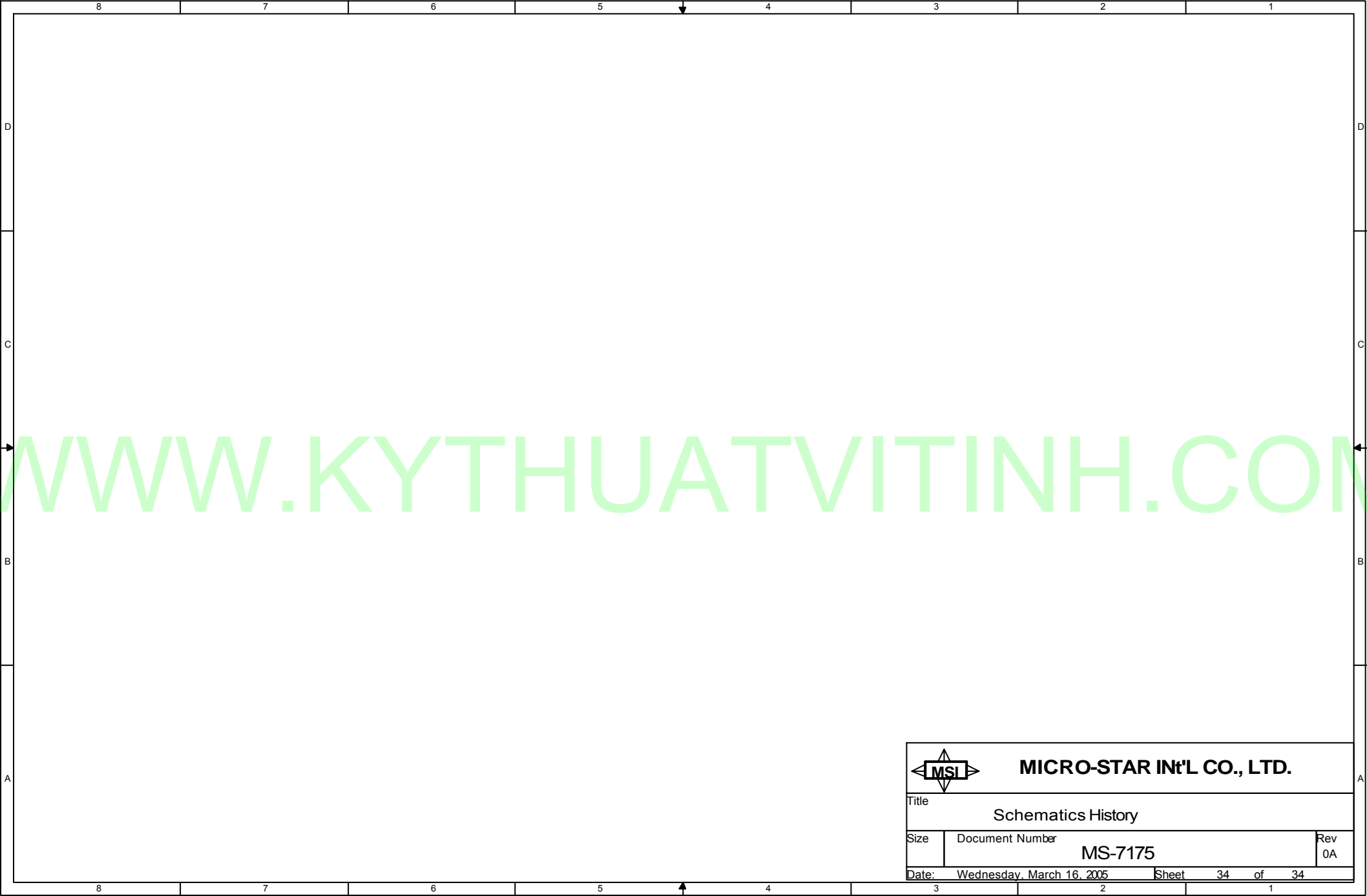
MICRO-STAR INT'L CO., LTD.			
Title POWER DELIVERY MAP & MANUAL PART			
Size	Document Number	Rev	
	MS-7175	0A	
Date: Wednesday, March 16, 2005	Sheet	31	of 34


PWROK MAP



RESET MAP





		MICRO-STAR INT'L CO., LTD.	
Title			
Schematics History			
Size	Document Number		Rev
	MS-7175		0A
Date:	Wednesday, March 16, 2005	Sheet	34 of 34